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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,553	05/18/2005	William Donaldson	US02 0454 US	7482

65913 7590 07/13/2009

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ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
07/13/2009	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WILLIAM DONALDSON and EDMOND TOY

Appeal 2009-002950
Application 10/535,553
Technology Center 2800

Decided:[1] July 9, 2009

Before JOHN A. JEFFERY, CARLA M. KRIVAK, and
KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-20 (Br. 2).[2] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

The Disclosed Invention[3]

Appellants' invention provides at least one switch control circuit for constraining electromagnetic emissions from a floating power transfer device such as a charge pump. The charge pump transfers power from a voltage source 107 to a capacitor CS, and then the capacitor CS transfers power to a floating data bus 214, 215 and a hold capacitor CH. The at least one switch control circuit 402, 411 enables the voltage transfer to the capacitors and floating data bus 214, 215 to control the emissions. A floating bus is one electrically isolated from ground through diodes or otherwise through switches. The switch control devices also constrain a slew rate on the floating bus to control the emissions. (Figs. 2, 4; Spec. 1:4-30, 4:14-15, 5:1-10).

The Claims

Exemplary claims 1, 7, 8, 9, and 13 follow:

> 1. A device comprising: a floating bus; a power and data system for driving the floating bus, the power and data system comprising a charge pump circuit; and at least one switch control circuit coupled to the floating bus and the power and data system for facilitating charging of the floating bus and for controlling electromagnetic emission from the device.
>
> 7. The device of claim 6, wherein the first switch control circuit and the second switch control circuit are driven by a

[2] Appellants' Brief (filed Jun. 19, 2007) ("Br.") and the Examiner's Answer (mailed Oct. 10, 2007) ("Ans.") detail the parties' positions.

[3] The description herein of Appellants' invention constitutes findings of fact.

reference circuit, the reference circuit generating a first reference signal for the first switch control circuit and a second reference signal for the second switch control circuit.

8. The device of claim 7, wherein when a voltage across a first terminal and a second terminal of the first switch control circuit is greater than a threshold value, output current from the first switch control circuit is constant at a value dependent on the first reference signal, and when voltage across a first terminal and a second terminal of the second switch control circuit is greater than the threshold value, output from the second switch control circuit is constant at a value dependent on the second reference signal.

9. The device of claim 1, wherein the at least one switch control circuit controls electromagnetic emission from the device by constraining the slew rate on the floating bus.

13. The circuit of claim 10, wherein the first switch control circuit and the second switch control circuit are each operable in at least a low speed mode and a high speed mode, with mode of the first switch control circuit and the second switch control circuit being determined by the first reference signal and the second reference signal generated by the reference circuit in response to an input control signal which is dependent upon a desired floating bus charging speed.

Prior Art and Rejections

Wang	US 6,087,857	Jul. 11, 2000
Buhring	EP 1065600 A2	Jan. 3, 2001[4]
Roman	US 6,204,649 B1	Mar. 20, 2001
Yamanaka	US 2002/0154524 A1	Oct. 24, 2002
Tomita	US 6,493,275 B2	Dec. 10, 2002 (filed Aug. 6, 2001)

[4] Throughout this opinion, the English translation of record (supplied by FLS, Inc. to the USPTO) listing "Buehring" as the inventor (*hereinafter* "Buhring") is referenced. Appellants and the Examiner also refer to the US counterpart to Buhring (US 6,710,626); however, as stated, reference here to "Buhring" denotes the translation.

Buhring US 6,710,626 B1 Mar. 23, 2004
(filed June 29, 2000)

DAVID J. COMER, MODERN ELECTRONIC CIRCUIT DESIGN 69-70 (1976).[5]

Claims 1-4, 6-12, 14-16, and 18-20 stand rejected as obvious under 35 U.S.C. § 102(b) based on Buhring.

Claims 5, 13, and 17 stand rejected as obvious under 35 U.S.C. § 103(a) based on Buhring and Yamanaka.

PRINCIPLES OF LAW

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). "[A]fter the PTO establishes a prima facie case of anticipation . . ., the burden shifts to appellant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied upon." *In re King*, 801 F.2d 1324, 1327 (Fed. Cir. 1986) (internal quotation marks omitted). "It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim." *Id.* at 1326. "A reference anticipates a claim if it discloses the claimed invention 'such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.'" *In re Graves*, 69

[5] Comer was not cited by the Examiner. Comer is cited as an evidentiary reference to show well-known MOSFET transfer curve characteristics implicit or inherent in known MOSFET devices. Tomita, Roman, and Wang were cited by the Examiner as evidentiary sources but are cumulative to findings in support of this opinion.

F.3d 1147, 1152 (Fed. Cir. 1995) (quoting *In re LeGrice*, 301 F.2d 929, 936 (CCPA 1962)) (emphasis deleted).

Under § 103, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Such a showing requires:

> "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

If the Examiner makes such a showing, the burden then shifts to Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *Oetiker*, 977 F.2d at 1445.

OPINION

Claims 1-4 and 6

Issue

Appellants argue against the anticipatory rejection of claim 1 (Br. 7, 8) by asserting that Buhring's circuit does not control electromagnetic emissions (EME). The issue before us is: Did Appellants demonstrate that the Examiner erred in finding that Buhring discloses "at least one switch

control circuit . . . for controlling electromagnetic emission from the device" as required by claim 1?[6]

Findings of Fact (FF)

Buhring

1. Buhring discloses a charge pump circuit employing voltage control signals from voltage sources 12, 13, 14, and 15 to control switching in transistors 7, 8, 9, 10, and 20. The "control signals" alternately separate a floating capacitor 6 from a voltage source while connecting it to a floating data bus (CAN_H, CAN_L), and vice versa, connecting the floating capacitor to a voltage source for charging the capacitor while separating the capacitor from the floating bus. (¶ 0031; Fig.).

2. The charge pump circuit decreases electromagnetic radiation caused by a data transmitter (undepicted), which switches states to impose data on the data bus (¶¶ 0001-08; 0031; Fig.). By employing the floating capacitor and the transistor switching scheme, "*there is* [not only] *a further reduction of the electromagnetic radiation* at the time of switching the states" (¶ 0004 (emphasis added)), but "*greatly reduced electromagnetic radiation*" at the time of the switching of the transmitter states (¶ 0008 (emphasis added)).

3. Buhring summarizes the pump circuit and transmitter operation as follows:

> In summary . . ., as a result of using the capacitor, which is alternatively charged by the voltage source or connected to the data bus, *the electromagnetic radiation can be reduced* during those times in which there is a transition from the active

[6] Appellants' arguments are directed to claim 1 (Br. 5-9). Accordingly, under 37 C.F.R. § 41.37(c)(1)(vii), claim 1 is selected to represent the group.

> to the passive state of the transmitter, or vice versa. This is achieved by not having a fixed potential impressed on the two lines 1 and 2 of the data bus in the active state of the transmitter, but by connecting them to the capacitor 6, which has a floating potential.

(¶ 0033 (emphasis added); Fig.).

Analysis

As the Examiner found, Buhring discloses a device that employs control signals 14, 15 to switch transistors 9, 10, and 20 for controlling electromagnetic emission (EME) (Ans. 7; FF 1-3). The alternate switching of the floating capacitor onto the data bus and the voltage source results in "*greatly reduced electromagnetic radiation*" (FF 2). As such, according to Appellants' definition of control (i.e., to "*exercise restraint or direction over; hold in check, or curb*") (Br. 8), Buhring's circuit controls the EME. Appellants disclose a similar circuit, which alternately switches a capacitor to data bus in which the data bus and capacitor float with respect to the source (*see supra* note 3). As such, Appellants' argument (Br. 6-8) that Buhring's circuit does not control such electromagnetic emissions lacks merit.

Conclusion

Appellants did not demonstrate the Examiner erred in finding that Buhring discloses "at least one switch control circuit . . . for controlling electromagnetic emission from the device" as required by claim 1. Therefore, we will sustain the Examiner's rejection of claim 1, and claims 2-4 and 6 not separately argued.

Claim 7

Issue

Appellants argue (Br. 8) that Buhring's "power supply is not a reference circuit, and power supply voltages that may be supplied to switching signal generators 14 and 15 are not 'reference ***signals***.'" The issue is: Did Appellants demonstrate that the Examiner erred in finding that signals from the Buhring's generators 14 and 15 constitute reference signals?

Finding of Fact (FF)

Buhring

4. Buhring's "voltage sources 12, 13, 14, and 15 . . . supply the control signals" to the gates of transistors 7, 8, 9, and 10 to switch them on and off (¶ 0031; Fig.). Each source is connected to ground at one end and through a resistor at the other end to one of the transistor 12, 13, 14, and 15 gates (Fig.).

Analysis

Appellants' argument (Br. 8-9) that Buhring's supply voltages are not signals is not persuasive of Examiner error. According to Buhring's description, power supplies 13 and 14 create "control signals" (FF 1, 4). It follows that such "control signals" constitute the recited "reference signals" of claim 7, because Buhring's signals control transistors 9 and 10 by virtue of their reference to another potential such as ground at the gates of the transistors (FF 4). In other words, voltage potentials are defined in terms of a reference potential. Therefore, the Examiner's finding (Ans. 7, 8) that Buhring discloses "reference signals," in light of Buhring's description of such signals as "control signals," undermines Appellants' argument (Br. 8-9)

that Buhring's signals are not "reference signals" because "they are not *signals* at all."

Conclusion

Appellants did not demonstrate that the Examiner erred in finding that signals from the Buhring's voltage generators 14 and 15 constitute reference signals.

Claim 8

Issue

Appellants' arguments (Br. 9-10) present the following issue: Did Appellants demonstrate that the Examiner erred in finding that when voltages across Buhring's first and second switch control circuits are greater than a threshold value, output from the first and second switch control circuits are constant at values respectively dependent on the first and second reference signals, as required by claim 8?

Findings of Fact (FF)

Comer

5. Comer's Fig. 2.52 is reproduced below:

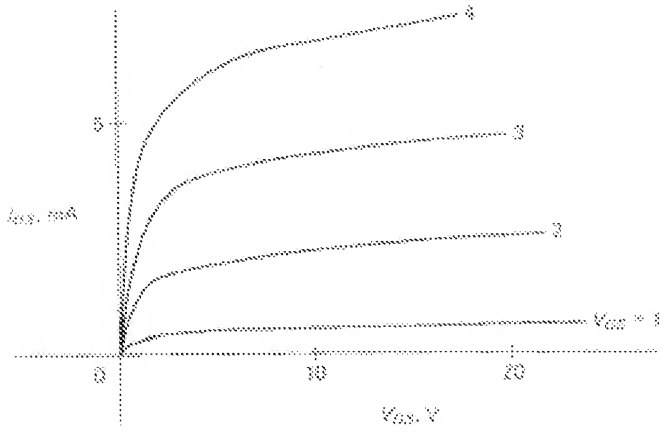

Fig. 2.52 depicts the typical V-I characteristics of an enhancement MOSFET (n-channel) device.

As seen in Comer's Fig. 2.52, with V_{GS} (gate to source) above a certain threshold voltage of about 1 volt, current I_{DS} through the MOSFET device is relatively constant for varying levels of V_{DS} (drain to source). "The channel resistivity is controlled by the gate-to-source voltage and generates the characteristics shown in Fig. 2.52." (Comer p. 69).

6. Comer's Fig. 2.54 is reproduced below:

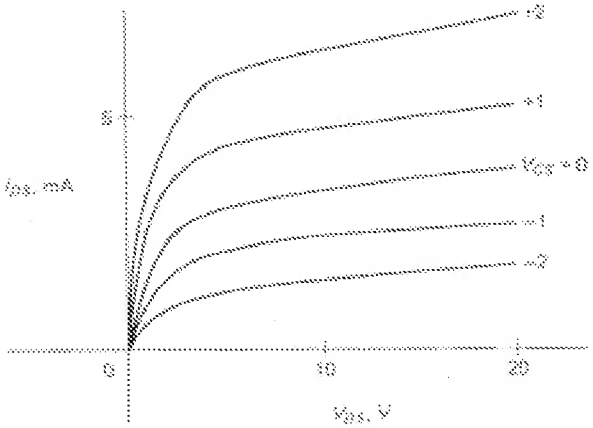

Fig. 2.54 depicts the typical V-I characteristics of a depletion/ enhancement MOSFET (n-channel) device. (Comer p. 70).

Buhring

7. Buhring's transistors 9, 10, and 20 are MOSFET transistors, preferably DMOS transistors ((¶¶ 0009, 0024, 0028-29). Buhring's circuit does not supply negative voltages; therefore, DMOS transistor 9 cannot turn on and supply current when V_{DS} is zero, as occurs during a short developed on the data bus lines. During such an undesired short, the DMOS transistor 20 turns on to supply current to the data bus that transistor 9 otherwise supplies in normal situations. (¶ 0028; Fig.).

Analysis

According to typical MOSFET curves, MOSFET transistors (including depletion mode MOSFETS, i.e., DMOS) require a certain

threshold voltage V_{DS} above zero volts across the drain to the source in order to conduct current. With such a voltage, a constant control voltage from the gate to the source V_{GS} generates a constant current I_{DS}. (FF 5, 6). Therefore, the typical MOSFET curves (*id.*) support the Examiner's finding (Ans. 4, 8) that each of Buhring's MOSFET/DMOS transistors 9, 10, and 20 constitute first and second switch control circuits requiring a threshold voltage (i.e., V_{DS}) such that when V_{DS} is greater than such a threshold value, output current I_{DS} from each of the first and second switch control circuits 9, 10, and/or 20 is constant at values respectively dependent on the first and second reference signals, i.e., signals at V_{GS} created from sources 14 and 15 (FF 1, 4, 7).

Appellants do not dispute the Examiner's findings with sufficient evidence or argument to demonstrate that Buhring's MOSFET/DMOS transistors and control circuits fail to meet the argued claim limitations. Appellants assert (Br. 9) that "a threshold value ***must*** be ***some*** value," but that assertion does not address the Examiner's finding (Ans. 8) that "zero (0)" constitutes "some" threshold value. Appellants also imply (Br. 9) that Buhring's output currents from transistors 9, 10, and 20 depend on the capacitor 6 voltage (Br. 9), but that implication does not address the Examiner's finding of additional current dependence on control signals from sources 14 and 15 creating V_{GS}. In other words, as is typical for MOSFETS, the output currents I_{DS} from transistors 9, 10, and/or 20 each depend on two different voltages, V_{GS} and V_{DS}, the latter of which corresponds to the recited voltage across first and second terminals being greater than a threshold voltage (and which includes the capacitor 6 voltage), and the

former of which corresponds to the recited first and second reference signals (*see* FF 4-7), thereby reasonably meeting the argued limitations of claim 8.

Conclusion

Appellants did not demonstrate that the Examiner erred in finding that when voltages across Buhring's first and second switch control circuits are greater than a threshold value, outputs from the first and second switch control circuits are constant at values respectively dependent on the first and second reference signals, as required by claim 8.

Claim 9

Issue

Appellants' arguments (Br. 10-11) present the following issue: Did Appellants demonstrate that the Examiner erred in finding that at least one of Buhring's switch control circuits control(s) "electromagnetic emission from the device by constraining the slew rate on the floating bus" as set forth in claim 9?

Finding of Fact (FF)

Appellants' Disclosure

8. Appellants' disclosure indicates that sharp voltage swings create electromagnetic emissions. Appellants' disclosure and Brief also indicate that constraining the slew rate means employing switches that avoid sharp current transitions such that current through each of Appellants' controlled switches does not abruptly transition from one value to another. (Br. 3; Spec. 7:5-14; Fig. 5).[7]

[7] Appellants' Brief (Br. 3) points to the cited passage at page 7 of their Specification as supporting the slew rate control limitation of claim 9.

Analysis

The Examiner found (*see* Ans. 8-9) that Buhring's transistors 9 and 20 constitute at least one switch control circuit that controls the electromagnetic emission by constraining the slew rate. The Examiner also found (Ans. 8), without rebuttal by Appellants, that "[t]he generated current determines the speed of the circuit, thus [it] determines the slew rate at the circuit's output or on the bus."

Buhring's transistor 20 maintains current flow to the data bus in the event of a short circuit between the data bus lines – in which case transistor 9 cannot provide such current (FF 7). Therefore, while Appellants and the Examiner disagree over whether Buhring's transistors 9 and 20 are on at the same time (Br. 10-11; Ans. 8-9), resolving this factual issue is not germane to the issue at hand, because, as indicated *supra*, there is no apparent disagreement that maintaining a supply of current to the data bus determines the slew rate on the bus–i.e., according to the Examiner's unrebutted finding (Ans. 8) quoted *supra* as bolstered by Appellants' disclosure (FF 8). Because transistor 20 does maintain such a current, it follows that transistor 20 in conjunction with transistor 9 avoids abrupt transitions, which would occur otherwise without transistor 20, thereby reasonably constraining the slew rate, according to Appellants' disclosure and arguments and the Examiner's findings (*see* FF 8).[8]

[8] "The problem in this case is that the appellants failed to make their intended meaning explicitly clear." *In re Morris*, 127 F.3d 1048, 1056 (Fed. Cir. 1997). "It is the applicants' burden to precisely define the invention, not the PTO's." *Id.*

Conclusion

Appellants did not demonstrate that the Examiner erred in finding that at least one of Buhring's switch control circuits control(s) "electromagnetic emission from the device by constraining the slew rate on the floating bus" as set forth in claim 9.

Claims 10-12, 14-16, and 18

With respect to independent claims 10, 14, and 18, Appellants (Br. 11-12) rely on arguments presented for claims 1, 7, and 9. Appellants do not present separate arguments with respect to dependent claims 11, 12, 15, and 16. Therefore, for reasons explained above with respect to claims 1, 7, and 9, Appellants have not demonstrated Examiner error in the rejection of claims 10, 14, and 18, and claims 11, 12, 15, and 16 not separately argued.

Claims 19 and 20

Claims 19 and 20 recite a similar "slew rate" limitation as that of claim 9, although claim 19 recites "adjusting a slew rate" instead of "constraining the slew rate." Claim 20 similarly recites a "slew rate adjusting means." The Examiner responded (Ans. 9) to Appellants' nominal arguments (Br. 13-14) against the rejections of claims 19 and 20 by stating that "Appellant addresses the same arguments regarding the rejections of claims 1, 7, 9. Therefore, the same responses are applied." Appellants do not dispute the Examiner's response as to the arguments being "the same."

As the Examiner reasoned, Appellants' arguments track their arguments against the rejection of claim 9, with Appellants relying primarily on the assertion (Br. 13-14) that transistors 9 and 20 are not on at the same time because transistor 20 is redundant to claim 9. Based on that assertion, Appellants argue there can be no slew rate adjustment (*id.*). However, for

reasons similar to those explained above with respect to claim 9, Buhring's redundant transistor 20 maintains the current flow when transistor 9 cannot, and thereby alters or adjusts the slew rate over what it otherwise would have been with only transistor 9 operating (FF 7).

In other words, in light of Appellants' disclosure (FF 8), and based on the respective arguments and Buhring's disclosure (FF 7), Buhring's transistor 20 reasonably adjusts the data bus slew rate because the transistor 20 maintains the current at a relatively constant value on the bus in the event of a data bus short, as compared to an abrupt current change or drop to zero that would otherwise occur without transistor 20 – because transistor 9 cannot supply such current during a data bus short.

Claims 5, 13, and 17

Issue

Did Appellants demonstrate that the Examiner erred in finding that Buhring and Yamanaka collectively teach high and low speed charging modes, with the charging modes of at least one switch control circuit being dependent on the desired floating bus charging speed?

Findings of Fact

Yamanaka

9. Yamanaka discloses two charging modes in a charge pump circuit, one with a relatively fast or normal duty cycle, and the other one with a slow duty cycle during start-up, so that a circuit connected to the voltage supply does not malfunction due to a rush current generated in the voltage supply on start-up of the voltage supply as it attempts to replenish the charging capacitor (¶¶ 0006-10; Abstract).

10. Yamanaka's pump and control circuit employs a control voltage feedback signal from the pump output 12 to generate either a low "L" (slow) or normal (fast) cycle charging signal rates at pump switches 2 for charging capacitor 3 based on the desired charging rate–which thereby depends on the control voltage at the output (Figs. 1, 3; ¶¶ 0020, 0024). Figure 3 depicts, *inter alia*, a voltage comparator circuit 11, 13, oscillation circuit 8, reference supplies 10, 19, comparator 15, and differentiating circuit 17 for controlling the two switch charge rate modes by generating the necessary voltage inputs to the pump circuit 2, 3 based on the feedback control voltage at output 12 as fedback to control circuit portion 11, 13 (*id.*). Yamanaka's circuits depicted at Figures 3-5 operate in similar fashions (¶¶ 0023-29).

Analysis

The Examiner finds that employing two charging rate modes in a charge pump circuit as Yamanaka teaches would have been obvious in a circuit such as Buhring's in order to reduce in-rush currents (Ans. 6-7). Appellants respond (Br. 14-15) by arguing that Yamanaka does not disclose a floating data bus so that the charging mode cannot be dependent on a "desired floating bus charging speed" as required by claim 5. Appellants' arguments fail to demonstrate error, because the Examiner's rejection is based on the combination of references, with Buhring disclosing the floating bus and Yamanaka disclosing the different desired charging speeds.

Appellants' related argument (Br. 15) that Buhring does not disclose a capacitor connected to ground that would generate a rush current also fails to demonstrate error. Appellants present no evidence that rush currents result only from a capacitor connection to ground or that Buhring's floating bus could not be inadvertently grounded. Moreover, Yamanaka teaches that

such rush currents are generated due to a lack of charge on the capacitor at start-up of the voltage supply (*see* FF 9). Such a teaching reasonably suggests application to pump circuits in general, including Buhring's pump circuit. Buhring also discloses problems with shorted bus lines (FF 7).

In addition, Buhring's pump charging circuit supplies power at its output to floating data bus lines (FF 1-3). Yamanaka's circuit protects similar outputs from rush currents on start-up of the power supply by measuring the voltage of the output and feeding it back to control the desired charging rate based on the feedback control voltage (FF 9, 10).

Appellants' further assertion (Br. 16), with respect to claim 13, that Yamanaka does not teach high and low speed modes determined by first and second reference signals generated by a reference circuit in response to an input control circuit, which is dependent on a desired floating bus speed, also fails to demonstrate error. As the Examiner generally found (*see* Ans. 9-10), Yamanaka's pump circuit generates a feedback voltage constituting "an input control signal," which, as supplied to the "reference circuit" 10, 11, 13, and 15 (FF 10), causes "first" and "second reference signal[s]," which determine the "low" and "high speed mode[s]"–(i.e., Yamanaka's slow and normal mode oscillation signals or signals causing those signals constitute the first and second reference signals (*see* FF 9, 10)) as "desired" to charge the output.

Appellants' further arguments against the rejection of claims 5, 13, and 17 (Br. 14-17) notwithstanding, Yamanaka's teachings suggest using different charging rate modes on any charge pump output such as Buhring's output floating data bus, as controlled under the Examiner's proposed modification (Ans. 9) by Buhring's floating data bus line voltage as

modified by Yamanaka's feedback control circuit (*see* FF 10). As noted *supra*, such control predictably reduces the in-rush current (FF 9; Ans. 6, 7), thereby suggesting the limitations of claims 5, 13, and 17.

Appellants' similar arguments (Br. 16-17) against the rejection of claim 17 track their arguments presented for claims 5 and 13. Similar to claim 13, Yamanaka's feedback circuit, *inter alia*, 8, 10, 11, 13, 15 (FF 10), constitutes a "reference generator" circuit controlling values of the first and second reference signal values, as set forth in claim 17–i.e., Yamanaka's feedback voltage from output 12 (at, e.g., comparator circuit 10, 11, 13) controls the reference circuit output to generate a slow (first reference value) and normal (second reference value) oscillation signal, which values then control the different charging rates as applied to switches 2 in pump circuit 2, 3. Yamanaka's pump switches 2 (FF 10) are similar to Buhring's pump switches 7, 8, 9, 10, and 20 (FF 1).

Thus, using Yamanaka's pump control technique in Buhring's pump circuit involves no "more than the . . . mere application of a known technique to a piece of prior art ready for the improvement," *KSR*, 550 U.S. at 417. "'Our suggestion test is in actuality quite flexible and not only permits, but requires, consideration of common knowledge and common sense.'" *Id.* at 421 (citation omitted) (emphasis omitted). Therefore, Appellants have not demonstrated Examiner error in the rejection of claims 5, 13, and 17.

Conclusion

Appellants did not demonstrate that the Examiner erred in finding that Buhring and Yamanaka collectively teach high and low speed charging

modes, with the charging modes of at least one switch control circuit being dependent on the desired floating bus charging speed.

DECISION

We affirm the Examiner's decision rejecting claims 1-20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

babc

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Notice of References Cited	Application/Control No. 10/535,553	Applicant(s)/Patent Under Reexamination William Donaldson et al.	
	Examiner Anh Quan Tra	Art Unit 2800	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
	A	US-				
	B	US-				
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	David J. Comer, Modern Electronic Circuit Design, Addison-Wesley Publishing Company 69-70 (1976).
	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

MODERN ELECTRONIC CIRCUIT DESIGN

DAVID J. COMER
California State University, Chico

ADDISON-WESLEY PUBLISHING COMPANY
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lead to a device that operates in the enhancement mode for a given polarity gate voltage and the depletion mode for the opposite polarity gate voltage.

Figure 2.51 shows an enhancement mode, n-channel MOSFET. The p-type substrate is of very high resistivity while the n-type source and drain are heavily doped. A thin oxide layer is formed over the substrate to protect the surface and to insulate the gate from the channel. Silicon nitride is used to shield the oxide layer from contamination. The metal gate is deposited so that it covers the entire region between the two n-regions.

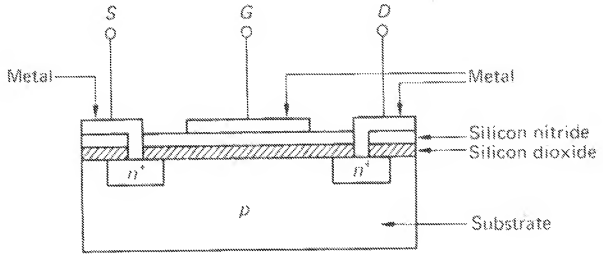

Fig. 2.51 Enhancement mode, n-channel-FET.

The metal gate and substrate act as the plates of a capacitance with the nitride and oxide acting as the dielectric. The substrate is often tied internally to the source terminal. A positive gate-to-source voltage results in positive charge collecting on the metal gate and an equal amount of negative charge induced near the surface of the substrate. This negative charge is present in sufficient quantity for relatively small gate voltages to convert the lightly doped p-material to n-type material. These free carriers induced near the substrate surface form an effective n-channel which conducts current from drain to source. The channel resistivity is controlled by the gate-to-source voltage and generates the characteristics shown in Fig. 2.52. The current limits near the drain end of the channel as the drain-to-gate voltage becomes positive enough so that negative charge is no longer induced in the channel. The governing equations are somewhat similar to those of the junction FET.

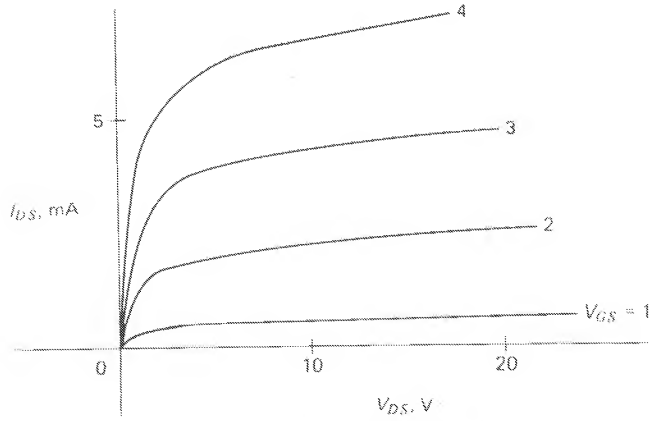

Fig. 2.52 V–I characteristics of enhancement MOSFET (n-channel).

The polarity of the gate voltage and drain voltage is the same for the enhancement mode MOSFET. A p-channel enhancement mode MOSFET can also be constructed that operates with negative values of V_{GS} and V_{DS}. For either of these MOSFET units, a zero value of gate voltage results in very small values of drain current. The junction FET conducts considerable current for the zero gate voltage condition and generally operates at lower current levels in practical applications.

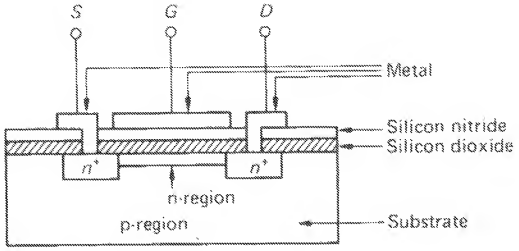

Fig. 2.53 A depletion/enhancement MOSFET (n-channel).

A second type of MOSFET can operate for both polarities of gate-to-source voltage. Figure 2.53 shows the depletion/enhancement MOSFET. This device is similar to the enhancement mode unit except that an n-region is added between the two heavily doped n-regions. A reasonable conductance now exists between source and drain even when the gate-to-source voltage is zero. A finite current flows from drain to source for $V_{GS} = 0$. If V_{GS} becomes negative, the n-channel contains fewer free carriers as the depletion region extends into the channel. The device behaves much like the junction FET for negative values of V_{GS}. When V_{GS} becomes positive, negative charge is induced in the n-channel and the conductivity is enhanced. If this MOSFET is properly designed, the characteristics for negative and positive values of V_{GS} are symmetrical enough to allow amplification with

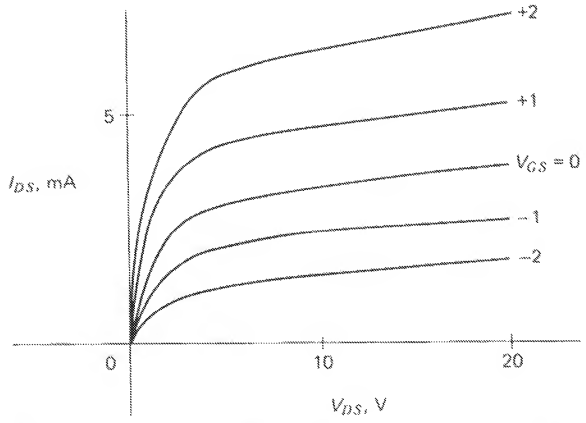

Fig. 2.54 V–I characteristics for the depletion/enhancement MOSFET (n-channel).

This book is in the
ADDISON-WESLEY SERIES IN ELECTRICAL ENGINEERING

Consulting Editors:
David K. Cheng
Leonard A. Gould
Fred K. Manasse

ISBN 0-201-01008-9
ABCDEFGHIJ-MA-798765